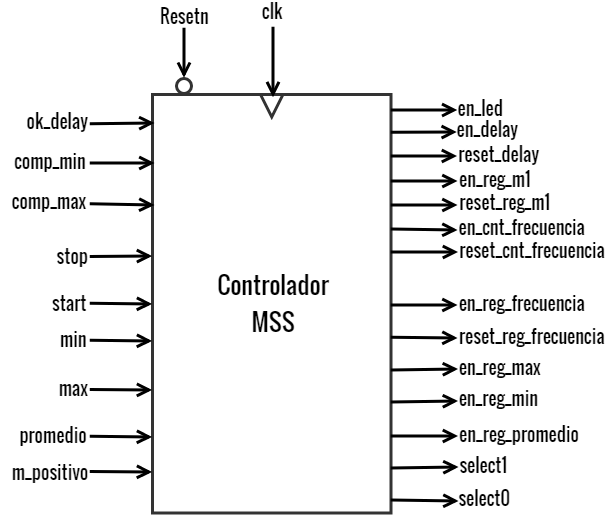
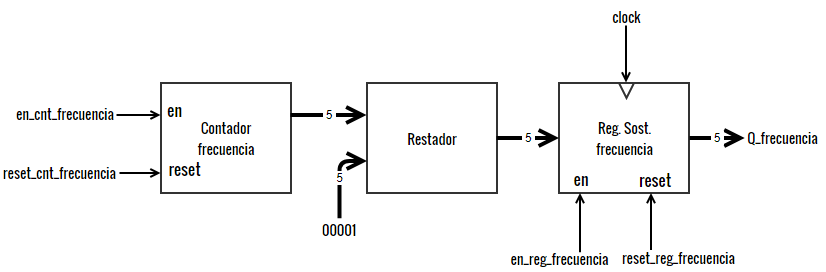
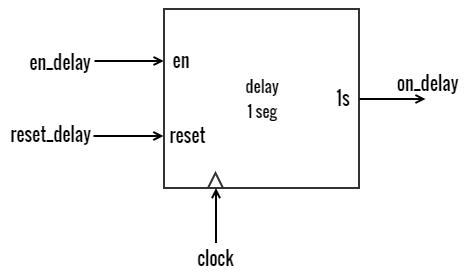
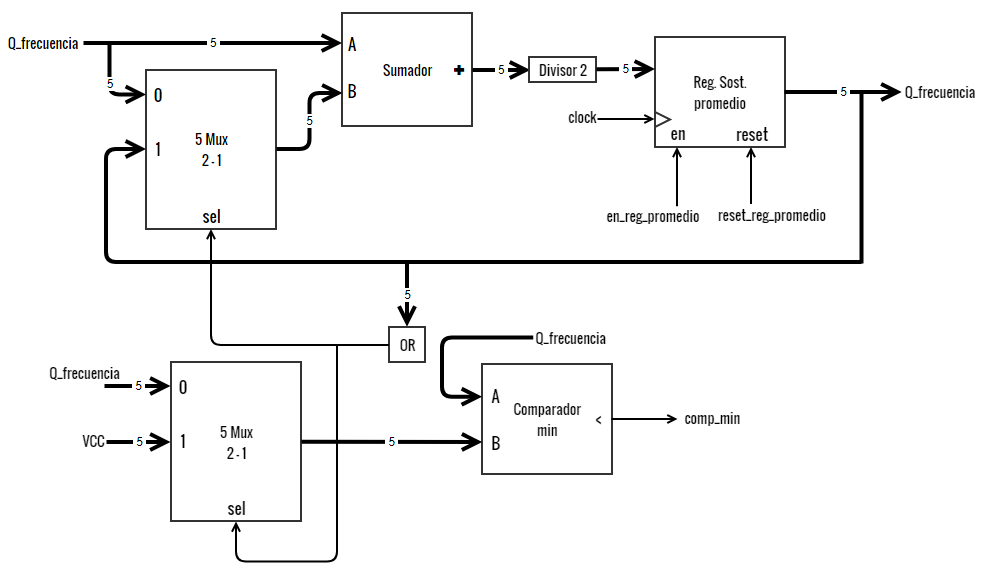
**Proyecto Sistemas Digitales II**

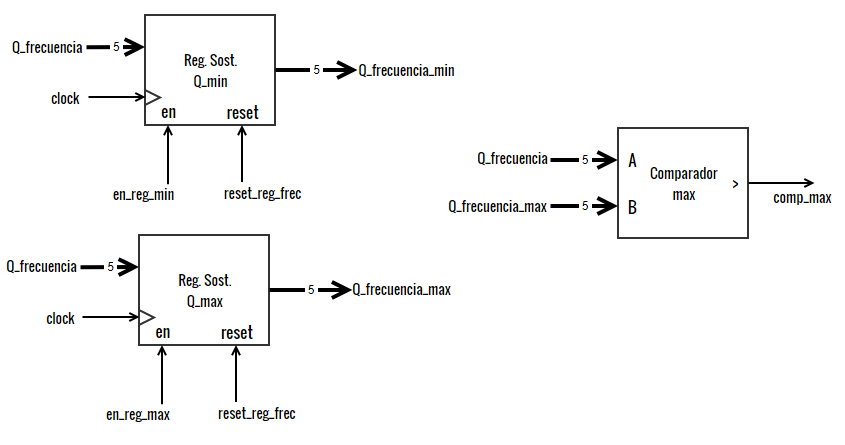
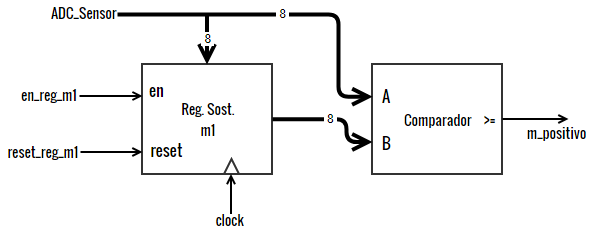
|  |  |  |
| --- | --- | --- |
| **Integrantes** | |  |
|  | Gilces Vargas Jimmy | |
|  | José Palominos | |

A continuación, se presenta el diagrama de bloques y partición funcional de la solución propuesta:

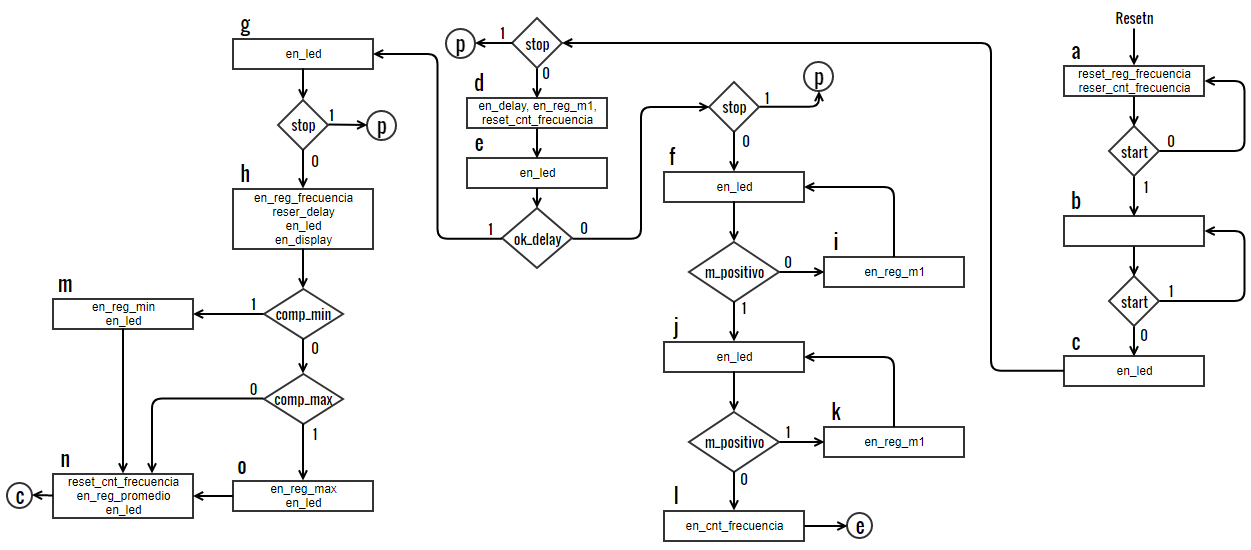


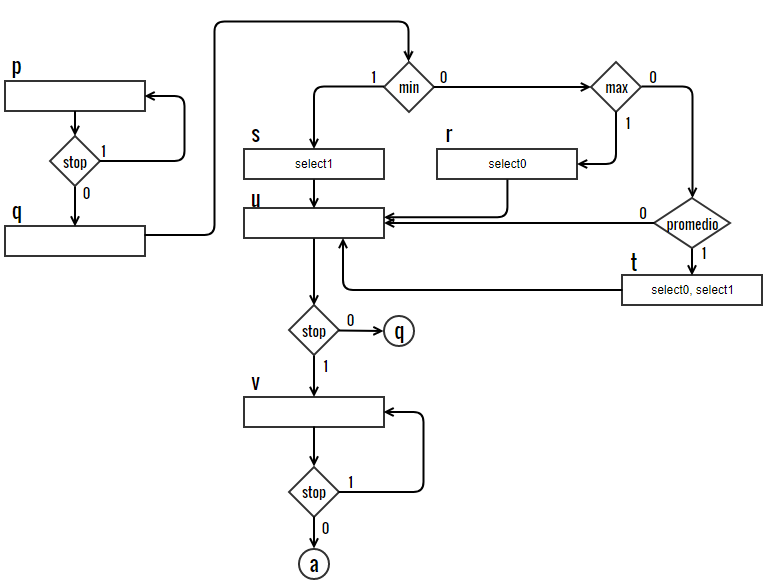






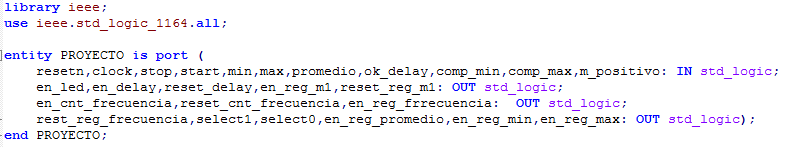
A continuación, se presenta el diagrama ASM del controlador:

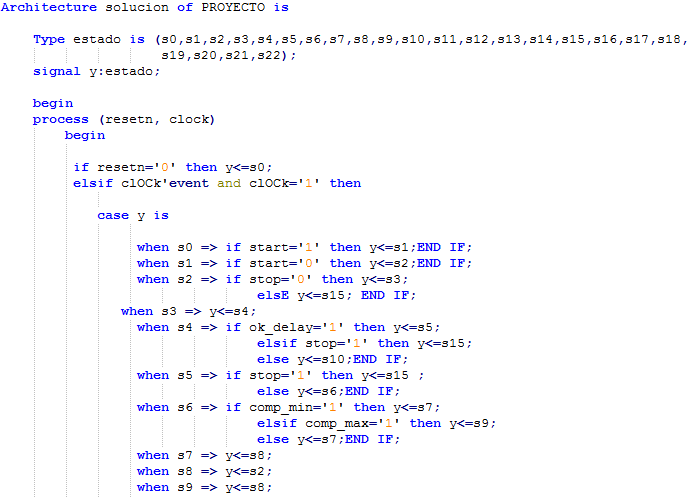


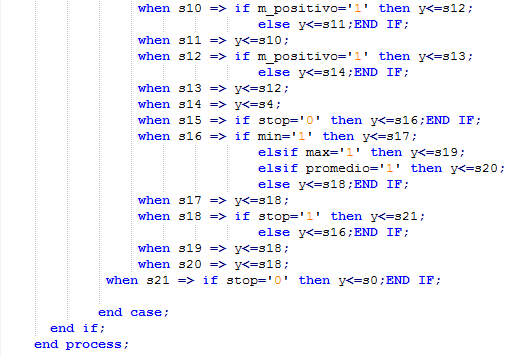


**Códigos VHDL de cada Bloque:**

CODIGO VHDL DEL CONTROLADOR:

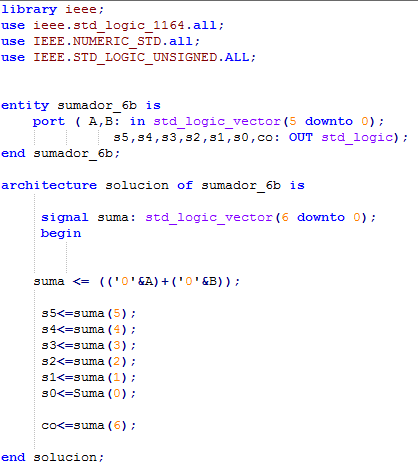




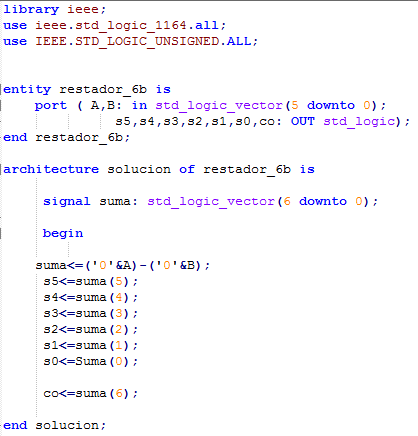




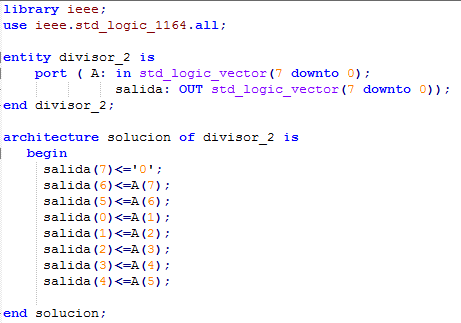
SUMADOR\_6B:



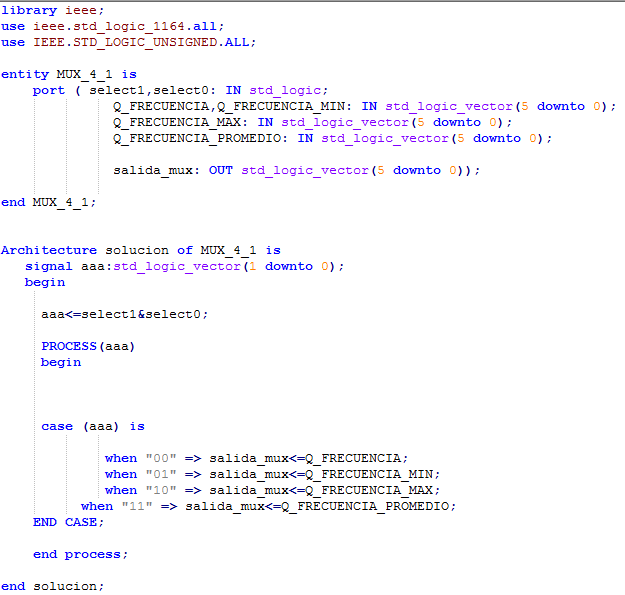
RESTADOR\_6B:



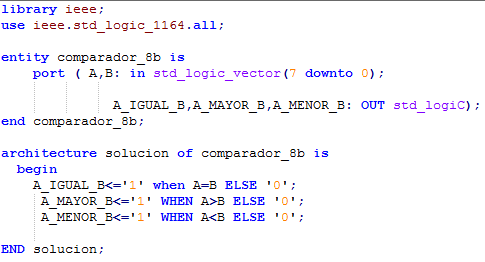
DIVISOR\_2:



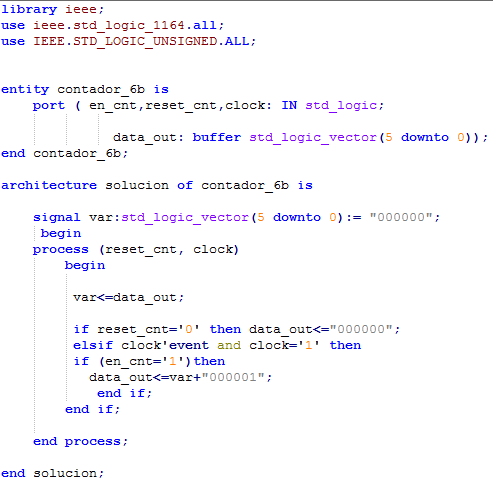
MUX\_4\_1\_



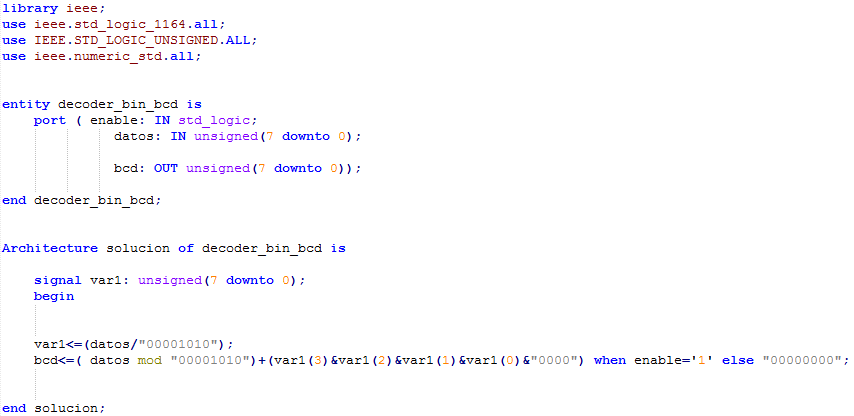
COMPARADOR\_8B:



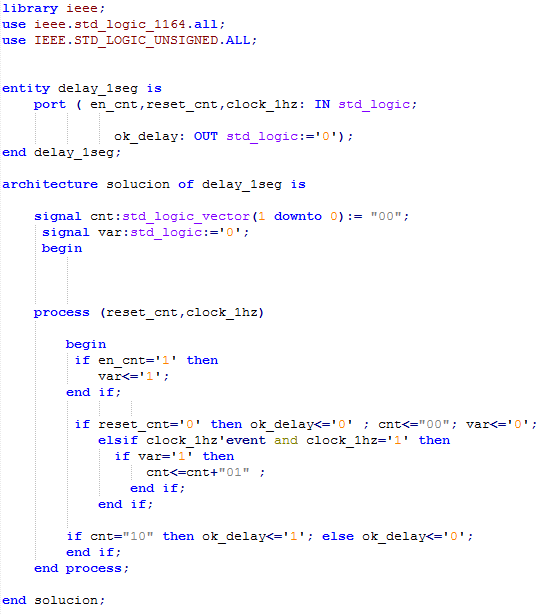
CONTADOR\_6B:



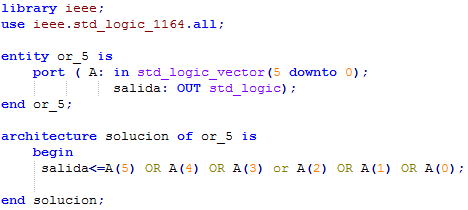
DECODER\_BIN\_BCD:



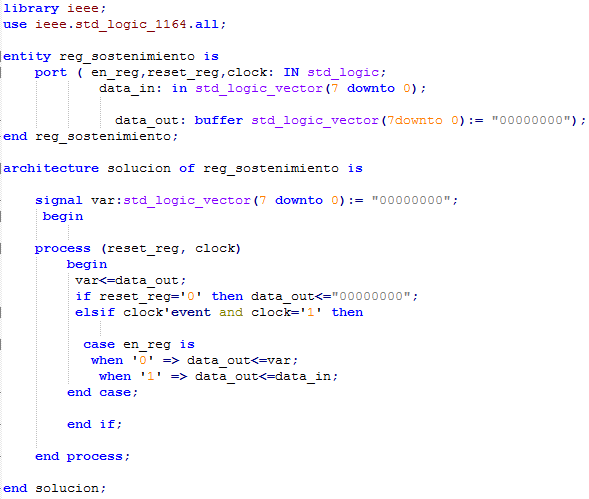
DELAY\_1SEG:



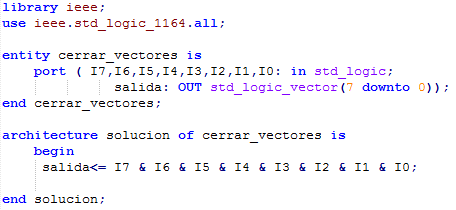
OR\_5:



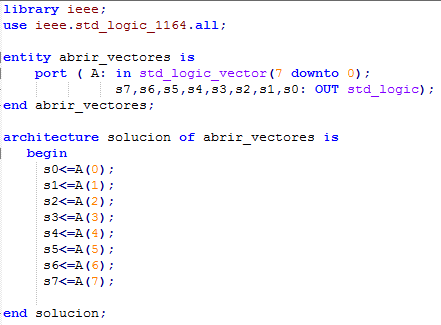
REG\_SOSTENIMIENTO:



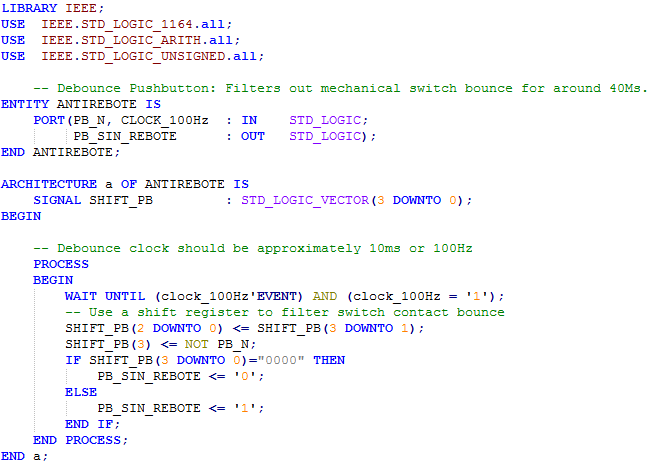
CERRAR\_VECTORES:



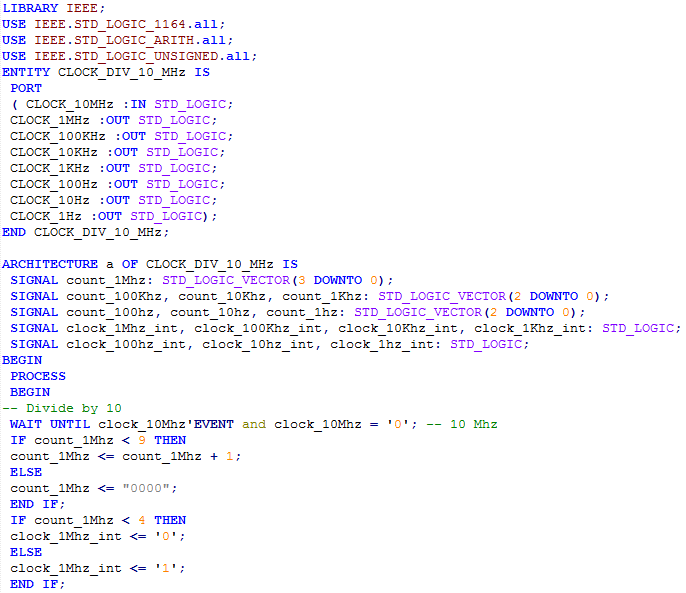
ABRIR\_VECTORES:

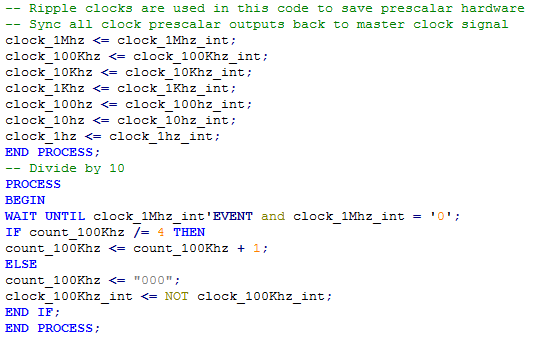


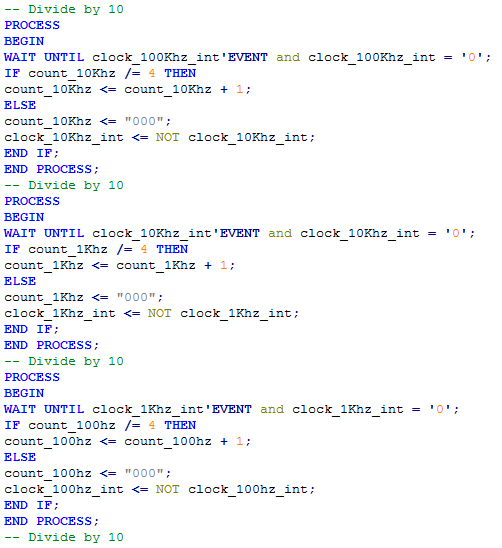
ANTIREBOTE:

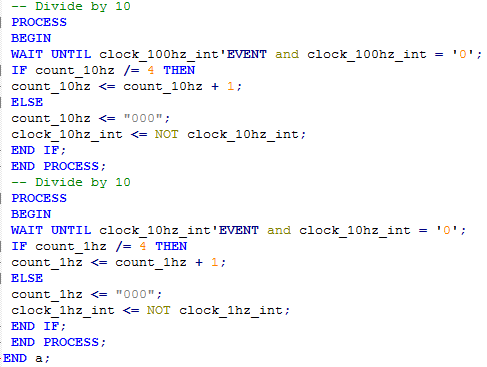


CLOCK\_DIV\_10\_MHz:

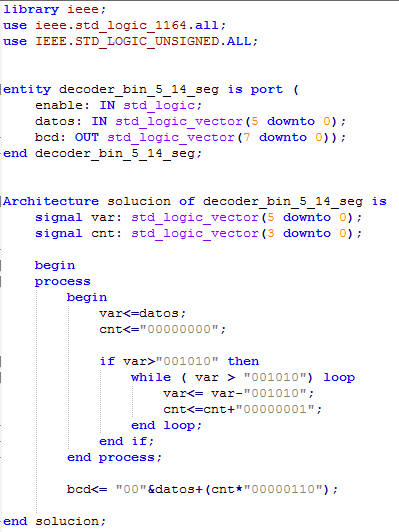


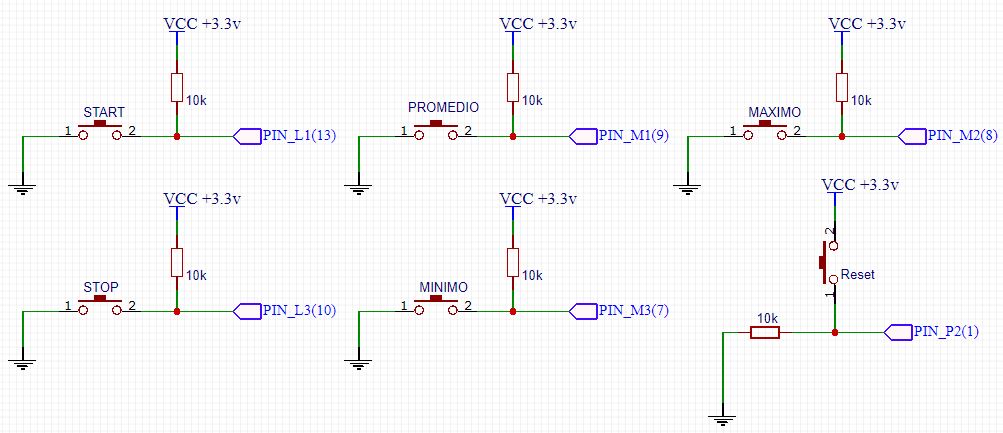


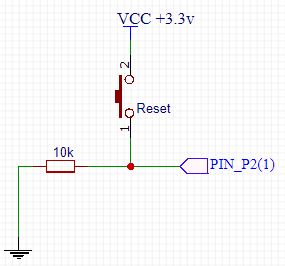
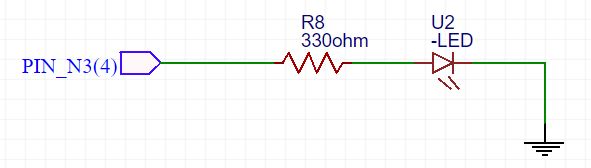
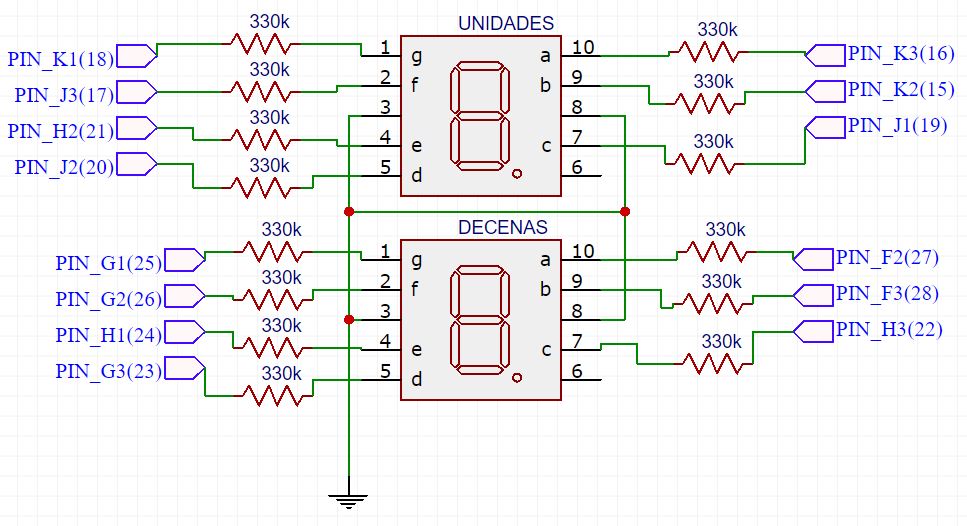


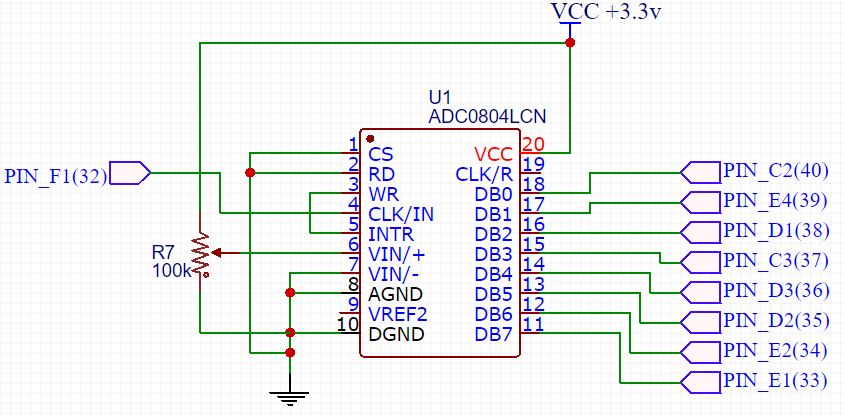
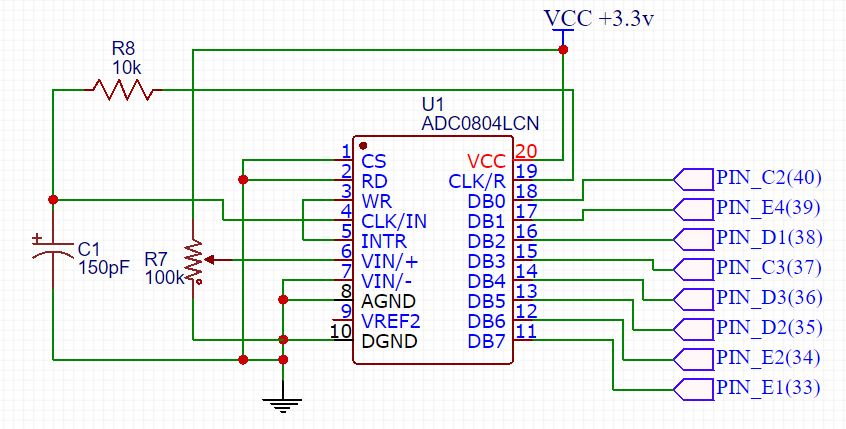


DECODER\_BIN\_5\_14\_SEG:



A continuación, se presenta el esquemático de los circuitos armados en protoboard, además se presenta la conexión hecha al C.I. 0804LNC.





**Conclusiones**

El Sistema Digital funciona correctamente de acuerdo al diagrama ASM propuesto.

Las altas frecuencias que se muestran en los displays pueden deberse a posibles fluctuaciones en el potenciómetro utilizado.

**Observaciones**